Please amend the claims as follows. This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-5 (previously cancelled)

Claim 6 (currently amended): A semiconductor device, comprising:

a substrate having transistor devices and a passivation layer disposed over a dielectric layer that is defined over the transistor devices;

a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by a porous dielectric material; and

a plurality of supporting stubs, each of the plurality of supporting stubs configured to form a supporting column that is disposed over a surface of the passivation layer and extends through the plurality of interconnect levels of the semiconductor device, the plurality of supporting stubs not being electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias so that the supporting column maintains structural contact with the passivation layer to avoid electrical contact with the plurality of copper interconnect metallization lines and conductive vias, the plurality of supporting stubs further being configured so as to not provide electrical connection between the plurality of interconnect levels of the semiconductor device .

Claim 7 (previously cancelled)

Claim 8 (currently amended): ~~A~~ The semiconductor device as recited in claim 6, further comprising:

a passivation-capping layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

Claims 9-25 (previously cancelled)

Claim 26 (currently amended): ~~A~~ The semiconductor device as recited in claim 6, wherein the plurality of copper interconnect metallization lines and conductive vias define dual damascene structures.

Claim 27 (currently amended): ~~A~~ The semiconductor device as recited in claim 6, wherein the plurality of supporting stubs further support a passivation-capping layer.

Claim 28 (currently amended): A semiconductor device, comprising:

a substrate having transistor devices;

an intermetal dielectric layer (ILD) including conductive contacts defining a first interconnect level of a plurality of interconnect levels of the semiconductor device;

a passivation layer defined over the ILD layer; and

a plurality of copper interconnect metallization lines and conductive vias defined in each remaining interconnect level of the plurality of interconnect levels of the semiconductor device defined over the passivation layer, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by only a porous dielectric material.

Claim 29 (currently amended): ~~A~~ The semiconductor device as recited in claim 28, further comprising:

a plurality of supporting stubs, each of the plurality of supporting stubs configured to form a supporting column that extends through each remaining interconnect level of the plurality of interconnect levels of the semiconductor device.

Claim 30 (currently amended): ~~A~~ The semiconductor device as recited in claim 29, wherein the plurality of supporting stubs is not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias.

Claim 31 (currently amended): ~~A~~ The semiconductor device as recited in claim 28, further comprising:

a passivation-capping layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

Claim 32 (currently amended): ~~A~~ The semiconductor device as recited in claim 28, wherein the plurality of copper interconnect metallization lines and conductive vias define dual damascene structures.

Claim 33 (currently amended): ~~A~~ The semiconductor device as recited in claim 29, wherein the plurality of supporting stubs further support a passivation-capping layer.

Claim 34 (currently amended): A semiconductor device, comprising:

a substrate having transistor devices;

an intermetal dielectric layer (ILD) including conductive contacts defining a first interconnect level of a plurality of interconnect levels of the semiconductor device, the conductive contacts being isolated from each other by a non-porous dielectric;

a passivation layer defined over the ILD layer; and

a plurality of copper interconnect metallization lines and conductive vias defined in each remaining interconnect level of the plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by one of only a porous dielectric material and a mixture of only a porous dielectric material and a gaseous dielectric; and

a passivation-capping layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

Claim 35 (currently amended): ~~A~~ The semiconductor device as recited in claim 34, further comprising:

a plurality of supporting stubs, each of the plurality of supporting stubs configured to form a supporting column that extends through each remaining interconnect level of the plurality of interconnect levels of the semiconductor device.